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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/967,240	09/28/2001	Sanu K. Mathew	884.448US1	6550

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EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 08/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/967,240	MATHEW ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *9/28/01;3 /25/02*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 15-16, 18-19, and 21-37* is/are rejected.

7)☒ Claim(s) *13,14,17 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) ✓
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/25/01*. ✓
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the applicant is advised to avoid using phrases "or the like is disclosed and claimed" in line 2. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-12, 15-16, 18-19, and 22-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Ashkenazi (U.S. 5,327,369).

Re claim 1, Ashkenazi discloses in Figures 3-4 an adder to sum two binary numbers (abstract as A+B+Cin), comprising: at least one circuit (40) adapted to generate

a group of carries; at least one sum generator (42) adapted to generate a pair of conditional sums (e.g. S_1 and S_0); at least one device (45) adapted to select between the pair of conditional sums and in response to one of the group of carries.

Re claim 2, Ashkenazi further discloses in Figures 2-4 at least one second circuit (41) adapted to generate additional carries missing from the group of carries to provide one carry for every group of a predetermined number of bits (8-bit group) of the two binary numbers.

Re claim 3, Ashkenazi further discloses in Figures 2-4 at least one second circuit is adapted to generate two conditional carries (P and G output from 41) for each additional carry (G only) and further comprising another device to select between the two conditional carries to provide each additional carry in response to one of the group of carries (30-37 in Figure 3A).

Re claim 4, Ashkenazi further discloses in Figures 2-4 the at least one device and the other device are each multiplexers (e.g. 46).

Re claim 5, Ashkenazi further discloses in Figures 2-4 a multiplexer recovery circuit coupled to each of the multiplexers (e.g. 46).

Re claim 6, Ashkenazi further discloses in Figures 2-4 at least one second circuit is all intermediate carry generator (output of 41).

Re claim 7, Ashkenazi further discloses in Figures 2-4 the at least one circuit is a sparse carry-merge circuit (40).

Re claim 8, Ashkenazi further discloses in Figures 2-4 an adder to sum two binary numbers (abstract as A+B+Cin) comprising: a sparse carry-merge circuit (40) adapted to

generate a first predetermined number of carry signals (P and G); a plurality of intermediate carry generators (41) each coupled to the sparse carry merge circuit and adapted to generate a second predetermined number of carry signals (output of 41); and a plurality of conditional sum generators (42) coupled to the sparse carry-merge circuit and the plurality of intermediate carry generators and adapted to provide the sum of the two binary numbers (46 and 45).

Re claim 9, Ashkenazi further discloses in Figures 2-4 the sparse carry-merge circuit merges groups of sixteen bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group (44).

Re claim 10, Ashkenazi further discloses in Figures 2-4 the sparse carry-merge circuit merges groups of eight bits of the two binary numbers and the first predetermined number of carry signals is one carry signal from each group (8-bit group in 41).

Re claim 11, Ashkenazi further discloses in Figures 2-4 the second predetermined number of carry signals is one carry signal for each group of four merged bits of the two binary numbers (41 as group of 4).

Re claim 12, Ashkenazi further discloses in Figures 2-4 the sparse-carry merge circuit includes a plurality of stages (e.g. 38 and 31), each stage (e.g. 38 and 31) including a plurality of carry-merge logic gates to combine adjacent output signals from a preceding stage to provide the first predetermined number of carry signals (e.g. Figure 3A).

Re claim 15, Ashkenazi further discloses in Figures 2-4 each of the plurality of intermediate carry generators comprises three stages of ripple-carry merge gates (Figure 3A for 8bit).

Re claim 16, Ashkenazi further discloses in Figures 2-4 each of the plurality of intermediate carry generators comprises a plurality of rail pairs (Figure 4 with G and P), one rail of each rail pair being adapted to generate a first conditional carry signal for a logic 0 carry being input to the intermediate carry generator (P) and another rail of each rail pair being adapted to generate a second conditional carry signal for a logic 1 carry being input to the intermediate carry generator (G).

Re claim 18, Ashkenazi further discloses in Figures 2-4 each intermediate carrier generator comprises a plurality of circuits to each generate a carry signal of the second predetermined number of carry signals, each of the plurality of circuits including: a first rail adapted to generate a first conditional carry (e.g. P into 43), a second rail adapted to generate a second conditional carry (G into 43); and a multiplexer (43) adapted to select between the first conditional carry (P) and the second conditional carry (G).

Re claim 19, Ashkenazi further discloses in Figures 2-4 each of the plurality of conditional sum generators comprises a plurality of stages of ripple carry-merge gates and exclusive OR gates (Figure 3B).

Re claim 21, Ashkenazi further discloses in Figures 2-4 a multiplexer recovery circuit (46) coupled to the sparse carry-merge circuit, each of the plurality of intermediate carry generators (43 and 44) and each of the plurality of conditional sum generators (45).

Re claim 22, it is a system claim of claim 8. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 23, it is a system claim of claim 9. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 24, it is a system claim of claim 10. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 25, it is a system claim of claim 11. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 26, Ashkenazi further discloses in Figures 2-4 each of the sum generators comprises: four dual rail sum circuits (42 and 45), each circuit providing one bit of a final sum (output of 45) and one rail generating a conditional sum for a logic 0 carry-in (S_0) and the other rail generating a conditional sum for a logic 1 carry-in (S_1); and a multiplexer (45 and 46) coupled to each dual rail sum circuit to select the one or the other rail in response to a one in four carry from the intermediate carry generator.

Re claim 27, it is a system claim of claim 21. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Re claim 28, Ashkenazi further discloses in Figures 2-4 method of adding two binary numbers (abstract as A+B+Cin), comprising: generating (output of 40) a first predetermined number of carries by merging bits of the two binary numbers; generating (41) a plurality of conditional carries for a logic 0 carry-in; generating (41) another plurality of conditional carries for a logic 1 carry-in; selecting (43 and 44) between each one of the plurality of conditional carries for a logic 0 carry-in and an associated one of

the other plurality of conditional carries for a logic 1 carry-in in response to a carry-in from the first predetermined number of carries to provide a second predetermined number of carries; generating (42) a plurality of conditional sums for a logic 0 carry-in; generating another plurality of conditional sums for a logic 1 carry-in; selecting (45) between each one of the plurality of conditional sums for the logic 0 carry-in and an associated one of the other plurality of conditional sums for the logic 1 carry-in in response to a carry-in from the first and second predetermined number of carries to provide a final sum of the two binary numbers (output of 45).

Re claim 29, it is a method claim of claim 9. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 30, it is a method claim of claim 10. Thus, claim 30 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 31, it is a method claim of claim 11. Thus, claim 31 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 32, Ashkenazi further discloses in Figures 2-4 recovering any discharged ones of the second predetermined number of carries or digits of the final sum (inherently).

Re claim 33, it is a method claim of claim 8. Thus, claim 33 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 34, Ashkenazi further discloses in Figures 2-4 forming the sparse carry-merge circuit comprises forming a plurality of stages, each stage including a plurality of

carry-merge logic gates to combine adjacent outputs from a preceding stage to provide the group of carries (e.g. Figure 3A).

Re claim 35, it is a method claim of claim 15. Thus, claim 35 is also rejected under the same rationale as cited in the rejection of rejected claim 15.

Re claim 36, Ashkenazi further discloses in Figures 2-4 forming each of the conditional sum generators comprises: forming four dual rail sum circuits (42 with S_1 and S_0); and forming a multiplexer coupled to each dual rail sum circuit (45).

Re claim 37, it is a method claim of claim 21. Thus, claim 37 is also rejected under the same rationale as cited in the rejection of rejected claim 21.

Allowable Subject Matter

5. Claims 13-14, 17, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,257,218 to Poon discloses a parallel carry and carry propagation generator apparatus for use with carry-look-ahead adders.

b. U.S. Patent No. 6,496,846 to Bradley discloses a conditional carry encoding for carry select adder.

c. U.S. Patent No. 6,269,386 to Siers et al. disclose an 3X adder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

August 20, 2004

TODD INGBERG
PRIMARY EXAMINER